REMARKS

Claims 1-14 are pending in the present application. Claims 1, 2, 3, 4 and 5 have been amended. No new matter has been added.

Drawing Objection

The drawing has been objected to under 37 C.F.R. § 1.84(o). A replacement drawing sheet is provided herewith. In this amendment, labels have been added to the registers 4, 14, comparators 6, 16, multiplexers 3, 13, and control logic block 8.

Each of the objections will now be addressed.

1. Standardized shapes of drawings. The Office Action objects to the drawings for not having standardized shapes for the registers, comparators, multiplexers and control blocks. Applicant is unaware of any PTO requirement regarding the shapes of elements in block diagrams. In fact, Rule 83(a) very specifically states that "conventional features disclosed in the description and claims, where their detailed illustration is not essential for a proper understanding of the invention, should be illustrated in the drawing in the form of a graphical drawing symbol or a labeled representation (e.g., ***a labeled rectangular box***)." 37 C.F.R. § 1.83(a), emphasis added. In this case, Applicant has complied with the rule by providing a labeled rectangular box. *See also*, Hellestrand, Fig. 16, element 1609, cited by the Examiner and showing a multiplexer is a labeled rectangular box. That being said, if the Examiner will provide additional guidance as to the desired shape, Applicant will provide a replacement drawing sheet consistent with that guidance.

2. *Connections between devices are unclear.* The Office Action states that it makes no sense that the input to the comparators is also connected to the multiplexers. Paragraph 24 of the specification is very clear on this question.

> From the data input 1 of the CLB 9, the resulting data are led via the input data bus 7 to the corresponding bus input of the first or second LUT 2; 12 and thus to the corresponding first bus input of the first or second comparator 6; 16. Simultaneously, these data are led in one part of the bit width of the input data bus 7 to the corresponding multiplexer control input of the first and/or second multiplexer 3; 13 and also to the first input of the CLB control logic 8. From the control input 10 of the CLB 9, the control data are led over the control data bus 7 to the second input of the CLB control logic 8.

3. *Control block.* The Office Action states that the control block (presumably CLB control logic 8) needs to be diagrammed in standardized form. Once again, Applicant is unaware of any standardized form for a control block but remains willing to modify the drawing upon receipt of guidance. The operation of the control logic block is clearly described in the specification and the specific implementation is a matter of design choice that would be clear to one of ordinary skill in the art.

4. *Input 10.* Input 10 illustrates a control input for the control logic block 8. "From the control input 10 of the CLB 9, the control data are led over the control data bus 7 to the second input of the CLB control logic 8." Par. [0024]. The specification never states that control input 10 is limited to a clock signal nor that the second input of the CLB control logic 8 is limited to a clock input.

5. *"The applicant desires a patent without detail of the invention is unacceptable."* Applicant respectfully submits that the drawings meet each and every rule required by the Patent Office. One of ordinary skill in the art, reading the specification and drawings would understand the details of the invention.

Section 101 Rejection

Claims 1-14 have been rejected under 35 U.S.C. § 101 for nonstatutory subject matter. Section 101 provides that a patent may be obtained for "any new and useful process, machine, manufacture or composition of matter." Claim 1 is directed to an arrangement that includes an input data node, a CLB control logic circuit, a look-up table, an input data bus, a multiplexer, a control input node and a register data bus. These are all tangible, concrete things. Similarly, claim 6 is directed to a logic circuit that includes a register, a comparator, a multiplexer and a control block and claim 11 is directed to means for performing a switching function, means for selecting at least a portion of the comparison data; and a CLB control logic circuit. Once again, these are tangible things.

The Office Action states that "[t]here is no real world practical purpose for such a hardware device stated with the application." Applicant strongly disagrees. The claimed invention provides a circuit that is useful, concrete and tangible.

The claimed invention is useful. For example, embodiments of the invention provide a solution to the problem of minimizing the use of area for configurable array blocks. Par. [0015]. As another example, one configuration shows its advantage in that for the implementation of more than one conditional branch in an LUT, an additional savings of hardware resources is achieved by reducing the required CLBs. Par. [0021].

Further, the invention is concrete and tangible. The claimed circuit recites very specific circuit elements such as an input data node, a CLB control logic circuit, a look-up table, an input data bus, a multiplexer, a control input node and a register data bus. These physical elements are repeatable, non-unpredictable, real world and non-abstract.

The Office Action then concludes that "[the claimed invention] is just a collection of circuits, which the applicant claims parallels a if-then-else branch." Applicant respectfully submits that if you remove the pejorative characterizations "just" and "applicant claims" the conclusion itself recites statutory subject matter. A collection of circuits that performs a task is patentable. To state otherwise is simply wrong. That is the law.

Section 112 Rejection

Claims 1-14 were rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

The Office Action states there is no need for a second comparator or a second multiplexer and there is not a need for the results of both multiplexers to go into the control box. First, Applicant notes that only claim 9 recites a second comparator and a second multiplexer and, therefore, this rejection clearly has no bearing on claims 1-8 and 10-14.

With respect to the questions raised in the Office Action, Applicant respectfully directs the Examiner's attention to Paragraph [0019], which states

> This special configuration of the solution according to embodiments of the invention shows its advantage in that for the implementation of more than one conditional branch in an LUT, an additional savings of hardware resources is achieved by reducing the required CLBs. In addition, here it is favorably guaranteed that the comparison data, which are stored in the LUT and which are required for processing with the CLB controller, are also simultaneously already available for further processing in typical multiplexers of a CLB. Therefore, additional hardware, which would otherwise be necessary, is likewise spared for each CLB that is used.

With respect to the rejection under the written description requirement, Applicant respectfully submits that the specification describes the claimed invention in sufficient

detail that one skilled in the art will reasonably conclude that the inventor had possession of the claimed invention. As stated in the MPEP, it is now well accepted that a satisfactory description may be in the claims or any other portion of the originally filed specification. MPEP § 2163. Since the claims are substantially unchanged from the originally filed, there can be no doubt that the inventor had possession of the claimed invention.

Conclusion

Applicant respectfully submits that the presently claimed invention meets all of the statutory requirements and respectfully requests that the case be passed to issuance.

Respectfully submitted,

/Ira S. Matsil/
Ira S. Matsil
Reg. No. 35,272
Attorney for Applicant

Date: August 16, 2007

SLATER & MATSIL, L.L.P.
17950 Preston Rd., Suite 1000
Dallas, TX 75252
Tel: 972-732-1001
Fax: 972-732-9218